

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 10/050,347
Filing Date January 15, 2002
Inventor Gurtej S. Sandhu et al.
Assignee Micron Technology, Inc.
Group Art Unit 2813
Examiner Schillinger, L.
Attorney's Docket No. MI22-1897
Title: Methods of Forming Transistors

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

JAN 17 2003

References -- See attached Form PTO-1449

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In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

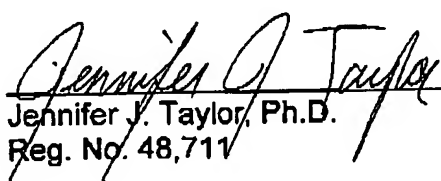
This Supplemental Information Disclosure Statement is being filed after the filing of the Request for Continued Examination (RCE) Application and before receipt of the first Office Action. Therefore, no fee is believed to be required. However, in the event that a fee is required for filing this Supplemental Information Disclosure Statement, please charge the fee specified under 37 C.F.R. §1.17(p) to Deposit Account No. 23-0925. Please credit Deposit Account No. 23-0925 with any overpayment of the above fee.

Citation of these references is respectfully requested.

Respectfully submitted,

Date:

1-16-2003


Jennifer J. Taylor, Ph.D.
Reg. No. 48,711

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Assistant Commissioner for Patents
Washington, D.C. 20231

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I hereby certify that the following papers are being facsimile transmitted to the Patent and Trademark Office at (703) 872-9318 on the date shown below:

1. Supplemental Information Disclosure Statement w/PTO-1449 and a copy of the cited reference

FEE DEFICIENCY

Although it is believed that no fees are due, the Commissioner is hereby authorized to charge any fees under 37 C.F.R. 1.16 and 1.17 which may be required by this paper to Deposit Account No. 23-0925.

Dated: January 17, 2003

By: Jaime M. White
Jaime M. White
Telephone No. (509) 624-4276
Facsimile No. (509) 838-3424

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